**Joseph Thornton**

**Sec 3: 5:30-6:45**

**Project 1 (Verilog)**

**Spring 2017**

**MERGED FILES**

a)

Script started on Sat 04 Mar 2017 04:14:12 PM PST

[thorntjl@athena:21]> cat proj1a.v

module proj1a(

input x,y,z,

output f

);

wire out1, out2, out3;

or o1(out1,x,y);

not n1(out2,y);

or o2(out3,out2,z);

and a1(f,out1,out3);

endmodule

[thorntjl@athena:22]> simv

Chronologic VCS simulator copyright 1991-2014

Contains Synopsys proprietary information.

Compiler version I-2014.03-2; Runtime version I-2014.03-2; Mar 4 16:15 2017

Joseph Thornton Section 3

X Y Z F

0 0 0

0

0 0 1

0 1 0

0 1 1

1

1 0 0

1 0 1

1 1 0

0

1 1 1

1

$finish called from file "proj1atest.v", line 34.

$finish at simulation time 8

V C S S i m u l a t i o n R e p o r t

Time: 8

CPU Time: 0.400 seconds; Data structure size: 0.0Mb

Sat Mar 4 16:15:03 2017

Script done on Sat 04 Mar 2017 04:15:17 PM PST

b)

Script started on Sat 04 Mar 2017 04:18:09 PM PST

[thorntjl@athena:22]> cat proj1b.v

module proj1b(

input x,y,z,

output f

);

wire out1, out2, out3;

nor o1(out1,x,y);

not n1(out2,y);

nor o2(out3,out2,z);

nor a1(f,out1,out3);

endmodule

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Compiler version I-2014.03-2; Runtime version I-2014.03-2; Mar 4 16:18 2017

Joseph Thornton Section 3

X Y Z F

0 0 0

0

0 0 1

0 1 0

0 1 1

1

1 0 0

1 0 1

1 1 0

0

1 1 1

1

$finish called from file "proj1atest.v", line 34.

$finish at simulation time 8

V C S S i m u l a t i o n R e p o r t

Time: 8

CPU Time: 0.410 seconds; Data structure size: 0.0Mb

Sat Mar 4 16:18:45 2017

Script done on Sat 04 Mar 2017 04:18:50 PM PST

C)

Script started on Sat 04 Mar 2017 04:20:11 PM PST

[thorntjl@athena:21]> cat proj1c.v

module proj1c

(

input x,y,z,

output f1,f2,r

);

assign f1 = x|y;

assign f2 = ~y|z;

assign r = f1&f2;

endmodule

[thorntjl@athena:22]> simv

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Compiler version I-2014.03-2; Runtime version I-2014.03-2; Mar 4 16:20 2017

Joseph Thornton Section 3

X Y Z F

0 0 0

0

0 0 1

0 1 0

0 1 1

1

1 0 0

1 0 1

1 1 0

0

1 1 1

1

$finish called from file "proj1atest.v", line 34.

$finish at simulation time 8

V C S S i m u l a t i o n R e p o r t

Time: 8

CPU Time: 0.230 seconds; Data structure size: 0.0Mb

Sat Mar 4 16:20:24 2017

Script done on Sat 04 Mar 2017 04:20:35 PM PST

d)

cript started on Sat 04 Mar 2017 04:21:23 PM PST

[thorntjl@athena:21]> cat proj1d.v

module proj1d

(

input x,y,z,

output reg f

);

always@(\*)

begin

case({x,y,z})

3'b000: begin f=0; end

3'b001: begin f=0; end

3'b010: begin f=0; end

3'b011: begin f=1; end

3'b100: begin f=1; end

3'b101: begin f=1; end

3'b110: begin f=0; end

3'b111: begin f=1; end

default: begin f=0; end

endcase

end

endmodule

[thorntjl@athena:22]> simv

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Contains Synopsys proprietary information.

Compiler version I-2014.03-2; Runtime version I-2014.03-2; Mar 4 16:21 2017

Joseph Thornton Section 3

X Y Z F

0 0 0

0

0 0 1

0 1 0

0 1 1

1

1 0 0

1 0 1

1 1 0

0

1 1 1

1

$finish called from file "proj1atest.v", line 34.

$finish at simulation time 8

V C S S i m u l a t i o n R e p o r t

Time: 8

CPU Time: 0.230 seconds; Data structure size: 0.0Mb

Sat Mar 4 16:21:37 2017

Script done on Sat 04 Mar 2017 04:21:41 PM PST

**ANALYSIS**

Truth table for function y=(x+y)(~y+z)

|  |  |  |  |
| --- | --- | --- | --- |
| X | Y | Z | F |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

4 **(see a,b,c,d above for test results)**test benches were run on all the above proj.v files with the same results matching the truth table shown above. Showing that all circuits were described correctly. **(code seen below)** note all test were run from same bench by simply changing the include and the compile time type.

module test1a();

reg x,y,z;

wire f1,f2,f;

proj1d a1(x,y,z,f);

initial begin

$display("\n\nJoseph Thornton Section 3\nX Y Z F");

$monitor(" %b",f);

x=0; y=0; z=0; $display("%b %b %b",x,y,z);

//test1

#1

x=0;y=0;z=1; $display("%b %b %b",x,y,z);

//test2

#1

x=0;y=1;z=0; $display("%b %b %b",x,y,z);

//test3

#1

x=0;y=1;z=1; $display("%b %b %b",x,y,z);

//test4

#1

x=1;y=0;z=0; $display("%b %b %b",x,y,z);

//test5

#1

x=1;y=0;z=1; $display("%b %b %b",x,y,z);

//test6

#1

x=1;y=1;z=0; $display("%b %b %b",x,y,z);

//test7

#1

x=1;y=1;z=1; $display("%b %b %b",x,y,z);

//test8

#1

$finish;

end

endmodule